WHAT IS CLAIMED IS:

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1. An apparatus comprising:

a first passgate circuit coupled to receive a first plurality of input signals and a first plurality of select signals, wherein the first passgate circuit includes a first output node, and wherein the first passgate circuit is configured to output a first voltage on the first output node responsive to an assertion of a first select signal of the first plurality of select signals, the first voltage indicative of a corresponding one of the first plurality of input signals; and

a first circuit coupled to receive the first plurality of select signals and coupled to the first output node, wherein the first circuit is configured to output a second voltage on the first output node responsive to each of the first plurality of select signals being deasserted.

2. The apparatus as recited in claim 1 further comprising:

a second passgate circuit coupled to receive a second plurality of input signals and a second plurality of select signals, wherein the second passgate circuit includes a second output node, and wherein the second passgate circuit is configured to output a third voltage on the second output node responsive to an assertion of a second select signal of the second plurality of select signals, the third voltage indicative of a corresponding one of the second plurality of input signals;

a second circuit coupled to receive the second plurality of select signals and coupled to the second output node, wherein the second circuit is configured to output a fourth voltage on the second output node responsive

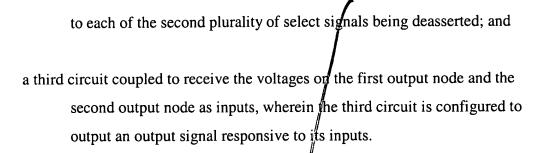
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- 3. The apparatus as recited in claim 2 wherein the second voltage represents a logical one, and wherein the third circuit performs an AND function on the voltages on the first output node and the second output node.
- 4. The apparatus as recited in claim 3 wherein the third circuit comprises a NAND gate.
- 5. The apparatus as recited in claim 2 wherein the second voltage represents a logical zero, and wherein the third circuit performs an OR function on the voltages on the first output node and the second output node.
- 6. The apparatus as recited in claim 5 wherein the third circuit comprises a NOR gate.
- 7. The apparatus as recited in claim 2 further comprising:

a third passgate circuit coupled to receive a third plurality of input signals and a third plurality of select signals, wherein the third passgate circuit includes a third output node, and wherein the third passgate circuit is configured to output a fifth voltage on the third output node responsive to an assertion of a third select signal of the third plurality of select signals, the fifth voltage indicative of a corresponding one of the third plurality of input signals;

a fourth circuit coupled to receive the third plurality of select signals and coupled to the third output node, wherein the fourth circuit is configured to output

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a sixth voltage on the third output node responsive to each of the third plurality of select signals being deasserted.

- 8. The apparatus as recited in claim 1 wherein the first circuit comprises a transistor and a logic gate.
 - 9. The apparatus as recited in claim 8 wherein the transistor is an N-type Metal-Oxide-Semiconductor transistor.
- 10. The apparatus as recited in claim 9 wherein the logic gate is a NOR.
 - 11. The apparatus as recited in claim 8 wherein the transistor is an P-type Metal-Oxide-Semiconductor transistor.
- 15 12. The apparatus as recited in claim 11 wherein the logic gate is an OR.
 - 13. The apparatus as recited in claim 1 wherein the first passgate circuit comprises a plurality of passgates, each of the plurality of passgates coupled to receive a respective one of the first plurality of select signals and a respective one of the first plurality of input signals, and each of the plurality of passgates coupled to the first output node.
 - 14. An apparatus comprising:
 - a first plurality of passgates, each coupled to receive a respective first input signal and a respective first select signal, and the plurality of passgates coupled to a first output node;
 - a first circuit coupled to receive the first select signals and coupled to the first output node, wherein the first circuit is configured to output a first voltage

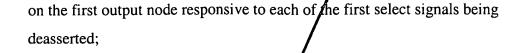
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- a second plurality of passgates, each coupled to receive a respective second input signal and a respective second select signal, and the plurality of passgates coupled to a second output node;
- a second circuit coupled to receive the second select signals and coupled to the second output node, wherein the second circuit is configured to output a second voltage on the second output node responsive to each of the second select signals being deasserted; and
- a third circuit having a first input coupled to the first output node and a second input coupled to the second output node, wherein the third circuit is configured to provide an output responsive to the first input and the second input.
- 15. The apparatus as recited in claim 1/4 wherein the first circuit comprises a transistor and a logic gate.
- 16. The apparatus as recited in claim 15 wherein the transistor is an N-type Metal-Oxide-Semiconductor transistor.
- 17. The apparatus as recited in claim 16 wherein the logic gate is a NOR.
- 18. The apparatus as recited in claim 15 wherein the transistor is an P-type Metal-Oxide-Semiconductor transistor.
- 19. The apparatus as recited in claim 18 wherein the logic gate is an OR.

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